Japanese Challenges for Multicore

Low Power High Performance Multicores, Compiler and API

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METI/NEDO National Project

Multi-core for Real-time Consumer Electronics

<Goal> R&D of compiler cooperative multi-core processor technology for consumer electronics like Mobile phones, Games, DVD, Digital TV, Car navigation systems.

<Period> From July 2005 to March 2008

<Features>  
• Good cost performance  
• Short hardware and software development periods  
• Low power consumption  
• Scalable performance improvement with the advancement of semiconductor 
• Use of the same parallelizing compiler for multi-cores from different vendors using newly developed API

API: Application Programming Interface

(2005.7～2008.3)**

**Hitachi, Renesas, Fujitsu, Toshiba, Panasonic, NEC
8 Core RP2 Multicore Designed to Support Compiler Optimization

<table>
<thead>
<tr>
<th>Process Technology</th>
<th>90nm, 8-layer, triple-Vth, CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Size</td>
<td>104.8mm²</td>
</tr>
<tr>
<td></td>
<td>(10.61mm x 9.88mm)</td>
</tr>
<tr>
<td>CPU Core Size</td>
<td>6.6mm²</td>
</tr>
<tr>
<td></td>
<td>(3.36mm x 1.96mm)</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.0V–1.4V (internal), 1.8/3.3V (I/O)</td>
</tr>
<tr>
<td>Power Domains</td>
<td>17 (8 CPUs, 8 URAMs, common)</td>
</tr>
</tbody>
</table>
8 SH4A Multicore RP2 Based on OSCAR Architecture

![Diagram of 8 SH4A Multicore RP2 Based on OSCAR Architecture]

LCPG: Local clock pulse generator
PCR: Power Control Register
CCN/BAR: Cache controller/Barrier Register
URAM: User RAM
Demo of NEDO Multicore for Real Time Consumer Electronics at the Council of Science and Engineering Policy on April 10, 2008

CSTP Members
Prime Minister: Mr. Y. FUKUDA
Minister of State for Science, Technology and Innovation Policy: Mr. F. KISHIDA
Chief Cabinet Secretary: Mr. N. MACHIMURA
Minister of Internal Affairs and Communications: Mr. H. MASUDA
Minister of Finance: Mr. F. NUKAGA
Minister of Education, Culture, Sports, Science and Technology: Mr. K. TOKAI
Minister of Economy, Trade and Industry: Mr. A. AMARI
OSCAR Parallelizing Compiler

• Improve effective performance, cost-performance and productivity and reduce consumed power
  – Multigrain Parallelization
    • Exploitation of parallelism from the whole program by use of coarse-grain parallelism among loops and subroutines, near fine grain parallelism among statements in addition to loop parallelism
  – Data Localization
    • Automatic data distribution for distributed shared memory, cache and local memory on multiprocessor systems.
  – Data Transfer Overlapping
    • Data transfer overhead hiding by overlapping task execution and data transfer using DMA or data pre-fetching
  – Power Reduction
    • Reduction of consumed power by compiler control of frequency, voltage and power shut down with hardware supports.
MTG of Su2cor-LOOPS-DO400

- Coarse grain parallelism PARA_ALD = 4.3
Power Reduction by Power Supply, Clock Frequency and Voltage Control by OSCAR Compiler

- Shortest execution time mode

- Realtime processing mode with deadline constraints
API and Parallelizing Compiler in METI/NEDO
Advanced Multicore for Realtime Consumer Electronics Project

Details of API: See http://www.kasahara.cs.waseda.ac.jp/

Sequential Application Program
(Subset of C Language)

API to specify data assignment, data transfer, power reduction control

Translate into parallel codes for each vendor

Executable codes for each vendor chip

Realtime Consumer Electronics Application Programs
Image, Secure Audio Streaming etc.

Waseda OSCAR Compiler

Proc0
Scheduled Tasks
Proc1
Scheduled Tasks
Proc2
Scheduled Tasks

T1 Stop
T2 T4
T3 T6 Slow

Backend compiler
API decoder Sequential Compiler

Backend Compiler
API decoder Sequential Compiler

Backend Compiler
API decoder Sequential Compiler

Data Transfer by DTC(DMAC)
Performance of OSCAR Compiler Using the Multicore API on Intel Quad-core Xeon

- OSCAR Compiler gives us 2.09 times speedup on the average against Intel Compiler ver.10.1
Performance of OSCAR Compiler Using the Developed API on 4 core (SH4A) OSCAR Type Multicore

3.31 times speedup on the average for 4cores against 1core
Processing Performance on the Developed Multicore Using Automatic Parallelizing Compiler

Speedup against single core execution for audio AAC encoding

* ) Advanced Audio Coding

![Diagram of processor cores](image.png)

- Numbers of processor cores

- Speedups

- 7.0
- 6.0
- 5.0
- 4.0
- 3.0
- 2.0
- 1.0
- 0.0

<table>
<thead>
<tr>
<th>Numbers of processor cores</th>
<th>Speedups</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.0</td>
</tr>
<tr>
<td>2</td>
<td>1.9</td>
</tr>
<tr>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td>8</td>
<td>5.8</td>
</tr>
</tbody>
</table>
Power Reduction by OSCAR Parallelizing Compiler for MPEG2 Decoding

MPEG2 Decoding with 8 CPU cores

Without Power Control
(Voltage: 1.4V)

With Power Control
(Frequency, Resume Standby: Power shutdown & Voltage lowering 1.4V-1.0V)

Average Power
Without Power Control: 5.73 [W]
With Power Control: 1.52 [W]

73.5% Power Reduction
Low Power High Performance Multicore Computer with Solar Panel

- Clean Energy Autonomous
- Servers operational in deserts